REMARKS

Applicants appreciate the courtesy extended by the Examiner during the interview of November 14, 2006. During the interview claim 1 was discussed along with the U.S. Patent No. 5,954,820 to Hetzler (hereinafter, "Hetzler"). No agreement was reached. The positions taken by the applicants are provided below. The positions taken by the Examiner were consistent with the final Office action.

This paper is responsive to a Final Office action dated August 21, 2006. Claims 1-10, 14-19, 21-24, and 26-28 were examined.

Claims 1 and 16 are objected to because of informalities. Those informalities have been corrected by way of the present amendment.

Claim 24 stands rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter. Claim 24 has been amended to address the § 101 rejection. Reconsideration of the rejection is respectfully requested in view of the amendment.

Claims 1-2, 4-5, 8-19, 21-24, and 26-28 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,954,820 to Hetzler (hereinafter, "Hetzler"). Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hetzler as applied to claims 1-2, 4-5, 8-19, 21-24, and 26-28 above. Claims 6-7 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hetzler as applied to claim 1-2, 4-5, 8-19, 21-24, and 26-28 and further in view of U. S. Patent No. 5,787,294 to Evoy (hereinafter, "Evoy").

With respect to claim 1, applicants respectfully traverse the rejection of claim 1 as anticipated by Hetzler. Even assuming that Hetzler teaches various power modes, SEEK/READ, IDLE, IDL2, and STANDBY, Hetzler does not teach *a plurality of performance states, including a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit* as explained below.

The Office action apparently relies on controller 56 as corresponding to the claimed integrated circuit. ("Hetzler teaches that utilization of controller 56 is dependent upon ... access of the CD-ROM drive itself.") The Office action further relies on Fig. 8 and col. 6, lines 41-64.

Fig. 8 shows three power levels, the SEEK/READ power P0, the IDLE power P1, and the mode power P2. Accesses at P0 consume the most power, P1 intermediate power and P2 the least power. It is also noted the IDLE power mode is the normal track-following operation when data is not being read and no seek is occurring. Hetzler uses the term "active state" to refer to the drive when it is in either the SEEK/READ or the IDLE modes. Hetzler also teaches that additional energy is consumed during read operations because more portions of controller electronics 56 are active. Hetzler, at col. 6, lines 30-32.

Hetzler teaches two common power-save modes referred to as IDLE2 and STANDBY. Hetzler, at col. 6, lines 32-55. In the IDLE2 mode, actuator 63 is parked and servo control electronics 53 and read electronics, including pre-amplifier and channel 54, are turned off to reduce power usage. In the STANDBY mode, the actuator 63 is moved to its parking location, and spindle motor 62 and spindle drive 51 are turned off. The STANDBY mode purportedly has all of the power savings of the IDLE2 mode, plus the additional reduction in power to spindle control electronics portion of controller 56 and spindle drive 51. Thus, applicants agree that Hetzler teaches that different power is consumed by controller 56 in various of the power modes.

However, Hetzler fails to teach that *a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit*. There is no teaching in Hetzler that the active states (SEEK/READ and IDLE) have different performance capabilities. In fact, applicants submit that it is reasonable to assume that the capabilities are identical. In contrast, applicants claim different performance capabilities for the claimed performance states (e.g., through different clock speeds and/or voltage levels – see claims 6, 7). The Office action states that "it should be apparent that when the CD-ROM drive jumps to the high power P0 state from either the lower power P1 or P2 state (as seen in Fig. 8), the power/performance mode of the controller 56 would change accordingly." Even if true, Hetzler does not teach different capabilities for P0 and P1 as explicitly required by the claim. Thus, with reference to Fig. 8 of Hetzler, while there is different power consumption between P0, P1, and P2, there is no teaching that the controller 56 has different performance capabilities in P0 and P1 as required by claim 1.

Nor does Hetzler teach elsewhere to skip all intermediate performance states between a current performance state and the maximum performance state (claim 2) each time the system determines that a higher performance state is required based on the determined utilization. In fact, Hetzler teaches in column 15, lines 30-32 that "once a power-save mode has been entered, it may be exited either by entering another power-save mode or by returning the component to an active state." Thus, applicants maintain that Hetzler fails to teach always going to the predetermined (or maximum performance state) as recited in claim 1 (or claim 2).

Hetzler also fails to teach that the change between the active states P1 and P0 is based on utilization of the integrated circuit (i.e., of what the Office action deems corresponds to the claimed integrated circuit – i.e., controller 56). Instead, the movement from P1 to P0 seems to be based on an access request. Nor is there a teaching that the movement from P2 to P0 is based on utilization of the integrated circuit, but instead, a density or frequency of access requests to the CD-ROM. That does not teach utilization of an integrated circuit.

Applicants further note that Hetzler further teaches in Fig. 5 that the power mode may be gradually increased (to greater performance) at step 309. In Fig. 5, the maxmode is the biggest power savings mode, so (mode-1) provides less power savings corresponding to more performance. Thus, Hetzler in Fig. 5 teaches away from the claimed invention of always going to a maximum performance mode (claim 2) if integrated circuit utilization indicates that a higher performance state is required.

With respect to claim 9, which recites that the integrated circuit includes a central processing unit, applicants respectfully submit Hetzler does not teach determining utilization of an integrated circuit including a central processing or determining that a higher performance state is required based on the determined utilization.

With regards to claim 10, Hetzler fails to teach a computing system having an integrated circuit with a maximum performance state and multiple lesser performance states in which the computing system is operable, each time the computing system determines that a higher performance state is required while in each of the multiple lesser performance states, to change to the maximum performance state, skipping any intermediate performance states between a current one of the multiple lesser performance states and the maximum performance state. As

pointed out above, Hetzler fails to teach, in Fig. 8 or elsewhere, going between active states P1 and P0 based on utilization of the integrated circuit (what the Office action deems corresponds to the claimed integrated circuit – i.e., controller 56).

With respect to claim 19, applicants respectfully submit, as pointed out above with respect to Fig. 8, that Hetzler also fails to teach that the change between the active states P1 and P0 is based on utilization of the integrated circuit (what the Office action deems corresponds to the claimed integrated circuit – i.e., controller 56). Thus, Hetzler fails to teach *while in each of the performance states other than a maximum performance state, changing from a current performance state to the maximum performance state, skipping all intermediate performance states between the current performance state and the maximum performance state, each time the computing system determines that a higher performance is required based on the determined utilization.* Accordingly, applicants respectfully submit that claim 23 and all claims dependent thereon distinguish over the references of record.

With respect to claim 23, applicants respectfully submit that Hetzler fails to teach a first and second instruction sequence as claimed. Specifically, Hetzler does not teach an instruction sequence operable to change from a lower processor performance state to the maximum performance state, skipping any performance state between the current state and the maximum state in response to each determination that a performance increase is required. As pointed out above Hetzler teaches with respect to Fig. 8 various power modes for a CD-ROM drive including a SEEK/READ power mode P0, the IDLE power mode P1, and the mode power P2 for a CD. However, those power modes do not correspond to the claimed processor performance states. Hetzler simply fails to teach an instruction sequence *operable to change from a lower processor performance state to the maximum performance state skipping any performance state between the current state and the maximum state in response to each determination that a performance increase is required.* Accordingly, applicants respectfully submit that claim 23 and all claims dependent thereon distinguish over the references of record.

Applicants also traverse the position taken in the Office action that "applicant's numerous predetermined performance states are construed to be an admission that the criticality does not reside in which performance state is entered and thus obvious variations of one another."

Applicants are making no such admission. The "numerous predetermined performance states" alluded to by the Examiner are (1) a maximum performance state in claim 2 and (2) a near maximum performance state in claim 3. If the Examiner believes the embodiment recited in claim 3 to be obvious over Hetzler, the Examiner is requested to provide a reference suggesting the modification to Hetzler to achieve the claimed invention. As of now, applicants respectfully submit that a prima facie case of obviousness has not been established for claim 3 and an indication of allowability of that claim is respectfully requested.

In summary, claims 1-10, 14-19, 21-24, and 26-28 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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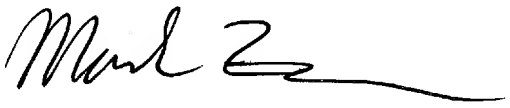

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